10/076966

ABSTRACT OF DISCLOSURE

Disclosed is a method and apparatus for an off boundary memory to provide off boundary memory access. The off boundary memory includes a right memory array having a plurality of right

5   memory rows and a left memory array having a plurality of left memory rows. This forms a memory having a plurality of row lines, each row line having a right memory row and a left memory row, respectively. An off boundary row address decoder is coupled to both the right and left memory arrays and is capable

10 of performing an off boundary memory access which includes accessing a desired plurality of memory addresses from one of a right or left memory row of a row line and from one of a left or right memory row of an adjacent row line at substantially the same time within one memory access cycle.